REMARKS

Claims 1-21 are currently pending in the application. No amendment is submitted with this response. In view of the arguments presented below, reconsideration of the rejection of claims 1-21 and allowance of the same are respectfully requested.

Claim Rejections – 35 U.S.C. § 103(a)

1. The Examiner has rejected claims 1-5, 8-12 and 15-19 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,163,828 to *Landi et al.* (*Landi*) in view of U.S. Patent No. 5,430,496 to *Silverbrook*. Applicants traverse this rejection.

As to the rejection of **claims 1, 8 and 15**:

The Examiner argues that *Landi* discloses a controller to "control the buffer (174 + 178) to selectively output the memory information (column 3 lines 36-44, Fig. 2, elements 120)." Office Action mailed 2-10-06, page 3. As described below, *Landi* teaches buffers connected to data ports of processors and memory; whereas the claimed invention recites a buffer coupled to insert terminals of DSPs and a memory. In *Landi*, multiplexers (130, 140, 150, 170) are engaged to couple CPU (105) and DSP (110) ports to corresponding ports on the memory (115). *Landi*: col. 3, ll. 36-44. Buffers (172, 174, 176, 178) permit two-way data transfer between the processors and memory, *Landi*: col. 3, ll. 33-35, and are employed only with respect to coupling CPU and DSP data ports to the memory data port, *Landi*: col. 3, ll. 45-54. *Landi* does not disclose buffers coupling to any other port of the memory. *See Landi*: Fig. 2.

In contrast, the claimed invention employs a buffer that couples the insert terminals of the DSPs to the insert terminal of the memory, as exemplified in Fig. 3. *Landi* discloses buffers (172, 174, 176, 178) employed only in combination with multiplexers (130, 140, 150, 170). *See Landi*: Fig. 2; and col. 3, ll. 36-54. In contrast, Applicants disclose buffers that are coupled only to insert terminals. *See* Applicants' Fig. 3, reference numeral 400 (buffers), lines 170, 270 and line to insert of memory 500. Applicants' claim 1 recites, inter alia, "a buffer coupled to an insert terminal of the memory and of each DSP"; Applicants' claims 8 and 15 recite, inter alia,

"the buffer being coupled to an insert terminal of the memory and of each DSP." *Landi* does not teach or suggest this limitation, and neither, as noted by the Examiner, does *Landi* teach or suggest a buffer coupled to insert terminals of the CPU and DSP and memory.

The Examiner argues that *Silverbrook* discloses a buffer being adapted to "output the [memory] insert signal to the insert terminal of each DSP . . . ," citing *Silverbrook*: col. 4, ll. 8-44 and Fig. 1A. *Silverbrook*, as described below, discloses a buffer as a bus protection device that is connected between a memory card bus 12 of the reader 10 and a processor bus 6 -- not a dedicated insert terminal of a memory or processor, as claimed by Applicants. Further, *Silverbrook* discloses a bus-based system wherein the buffer memory couples a memory card 17 to the processor bus 6 so that the memory card 17 does not "interfere with the logic levels of the processor bus [6]." *Silverbrook*: col. 4, ll. 8-12. In *Silverbrook*, the insertion or removal of a memory card is communicated to the host processor via pins within a memory card interface socket. That is, "[t]he memory card interface socket 10 is provided with short card detect pins which generate insertion and removal interrupts for the indication of the presence or otherwise of a memory card 17." *Silverbrook*: col. 4, ll. 20-24. A serial controller then relays a general interrupt to the host processor via the bus 6. *Silverbrook*: col. 4, ll. 24-31. Thus, *Silverbrook* contains no teaching of a processor or a memory having an insert terminal to which the buffer couples, as claimed by Applicants. Accordingly, *Silverbrook* provides no teaching or motivation to modify *Landi*, as suggested by the Examiner.

Because *Landi* and *Silverbrook*, either alone or in combination, fail to teach or suggest one or more limitations recited by Applicants' claims 1, 8 and 15, for at least this reason, Applicants' claims 1, 8 and 15 patentably distinguish from *Landi* and *Silverbrook* and are allowable over the references.

As to the rejection of **claims 2-5, 9-12 and 16-19**:

Claims 2-5 depend from independent claim 1; claims 9-12 depend from independent claim 8; and claims 16-19 depend from independent claim 15. Because independent claims 1, 8 and 15 are allowable over the cited prior art, for at least this reason, claims 2-5, 9-12 and 16-19 are also allowable as being dependent from an allowable base claims.

2. The Examiner has rejected claims 6-7, 13-14 and 20-21 under 35 U.S.C. § 103(a) as being unpatentable over *Landi* in view of *Silverbrook* in further view of U.S. Patent Application No. 2003/0020814 by *Ono*. Applicants traverse this rejection.

As to the rejection of **claims 6-7, 13-14 and 20-21**:

Claims 6-7 depend from independent claim 1; claims 13-14 depend from independent claim 8; and claims 20-21 depend from independent claim 15. Because independent claims 1, 8 and 15 are allowable over the cited prior art, for at least this reason, claims 6-7, 13-14 and 20-21 are also allowable as being dependent from an allowable base claims.

Conclusion

In view of the amendments and arguments set forth above, Applicants submit that the present application is in condition for allowance and would appreciate early notification of the same.

Invitation for a telephone interview

The Examiner is invited to call the undersigned at (202) 659-9076 if further issues remain with allowance of this case.

Deposit Account Authorization

Although no fee is believed due by submission of this paper, authorization is hereby made to charge any fees due or outstanding, or credit any overpayment, to Deposit Account No. **18-2220** (Order No. 45533).

Respectfully Submitted,

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